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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
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| 2837 | |

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/687,155 | FLOCK, HORST | |
| | Examiner | Art Unit | |
| | Patrick Miller | 2837 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *18-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-27 and 29-33* is/are rejected.

7)☒ Claim(s) *28 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01032005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 19, 20, 29, and 30 are objected to because of the following informalities: see bullet(s) below. Appropriate correction is required.

   - With respect to claims 19, 29, and 30, please remove the quotes ("").

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 18, 19, 21, 25, 27, 29, 30, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Fucili et al (5,886,484).

   - With respect to claims 18 and 19, Fucili et al disclose a control circuit (Fig. 2, 'Bridge_Control'), processor (Fig. 2, 'Signal_Control'), and half-bridge (Fig. 2, switches #2 and #3), used for operating an electric motors (Fig. 2, 'M'); the half-bridge including a first electronic switch between the supply voltage and a phase tap (Fig. 2, #2); a second electronic switch lying between the phase tap and ground (Fig. 2, #3); the control circuit controls the first and second switches with one out of only three switching signal pairings, where the three signal pairings are (1) the first switch on and the second switch off, (2) the first switch off and the second switch on, (3) both switches off (col. 4, ll. 1-17); and the processor has a signal output port coupled to the control circuit to select one

of the three signal pairings, via one of three possible output signals at the output port (Fig. 2, since the claim does not recite the output port having only one output, the Examiner has interpreted the output port of Fucili et al as comprising a first signal output, 'Bridge_ON' and a second signal output 'Bridge_TRISTATE,' where the first signal output can be "high" or "low" and the second signal output is "tristate," thus making only three possible output signals; also note that that if both transistors are turned on (#2 and #3), the transistors would become damaged).

- With respect to claim 21, Fucili et al disclose the control circuit comprising a stage that is not freely programmable (Fig. 2, 'Bridge_Control' is logic circuitry, which is can be in terms of integrated circuit chips, which are not freely programmable).
- With respect to claim 25, Fucili et al disclose the control circuit having two complementary stages that are controllable via the signal output port (Fig. 2, stage for switches #2 and #3 and stage for #1 and #4, and controlled by the 'Signal_Control').
- With respect to claim 27, Fucili et al disclose a driver circuit for each of the electronic switches (Fig. 2, separate outputs of the 'Bridge_Control' for each switch, #s 1-4, respectively).
- With respect to claims 29 and 30, Fucili et al disclose a tristate signal at the output port of the processor, which switches off the first and second switches (col. 4, ll. 15-17). Furthermore, tristate, by definition, means "floating."
- With respect to claim 32, Fucili et al disclose a control device for a load fed via phase taps of at least two half-bridges, each of the half-bridges being controllable with a control of its own (Fig. 2, 'Bridge_Control' output lines to each set of switches (#s 2, 3 and #s 1,

4) is interpreted to mean each side of the half-bridge has its own group of control lines); each control comprising: a first electronic switch between the supply voltage and a phase tap (Fig. 2, #2 and #1); a second electronic switch between the phase tap and ground (Fig. 2, #3 and #4); a control circuit that controls the first and second switches, with one of only three switching signal pairings for the two electronic switches (Fig. 2, 'Bridge_Control'), and where the signal pairings are (1) the first switch on and the second switch off, (2) the first switch off and the second switch on, (3) and both switches off (col. 4, ll. 1-17); and the control device comprising: a processor having a common signal output port coupled to control the controls via the respective control circuit of each control to select one of the three switching signal pairings, via one of three possible output signals at the common signal output port (Fig. 2, since the claim does not recite the output port having only one output, the Examiner has interpreted the output port of Fucili et al as comprising a first signal output, 'Bridge_ON' and a second signal output 'Bridge_TRISTATE,' where the first signal output can be "high" or "low" and the second signal output is "tristate," thus making only three possible output signals; also note that that if both transistors are turned on (#2 and #3), the transistors would become damaged).

- With respect to claim 33, the half-bridges are controllable by pulse-width modulation (Fig. 4, 'PWM' signal to 'FF-SR1' controls the bridges).

3. Claims 18, 21, 25, 27, 29, 30, 31, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Genova et al (6,534,937).

- With respect to claim 18, Genova et al disclose a control circuit (Fig. 1, #13), processor (Fig. 1, #12), and half-bridge (Fig. 1, Dm1 & Dm2), used for operating an electric

motors; the half-bridge including a first electronic switch between the supply voltage and a phase tap (Fig. 1, Dm1); a second electronic switch lying between the phase tap and ground (Fig. 1, Dm2); the control circuit controls the first and second switches with one out of only three switching signal pairings, where the three signal pairings are (1) the first switch on and the second switch off, (2) the first switch off and the second switch on, (3) both switches off (cols. ½, ll. 60-67/1-2); and the processor has a signal output port coupled to the control circuit to select one of the three signal pairings, via one of three possible output signals at the output port (Fig. 1, output of #12, INA to #13 produces three different "levels" that make #13 control the switches, Dm1 & Dm2 operate in one of the three signal pairings; also note that if both transistors are turned on, the transistors would become damaged. Therefore, Genova et al disclose only three signal pairings).

- With respect to claim 21, Genova et al disclose the control circuit comprising a stage that is not freely programmable (Fig. 1, #12 is decoding logic, which is can be in terms of integrated circuit chips, which are not freely programmable).
- With respect to claim 25, Genova et al disclose the control circuit having two complementary stages that are controllable via the signal output port (Fig. 1, stage for Dm1 and for Dm2 for phase A and stage for Dm1 and Dm2 for phase B, controlled by output from #12).
- With respect to claim 27, Genova et al disclose a driver circuit for each of the electronic switches (Fig. 1, separate outputs of #13 for each switch, Dm1 and Dm2, respectively).

- With respect to claims 29 and 30, Genova et al disclose a tristate signal at the output port of the processor, which switches off the first and second switches (col. 2, ll. 1-2). Furthermore, tristate, by definition, means "floating."
- With respect to claim 31, Genova et al disclose the control circuit having a driver circuit for each electronic switch (Fig. 1, #13 has two outputs, one for each switch, which is interpreted as separate drivers), and the driver circuit of the second electronic switch is capable of automatically switching the second switch into a freewheeling state in response to the inductance of a load coupled to the switch and switching off of the first electronic switch (col. 2, ll. 60-66).
- With respect to claim 32, Genova et al disclose a control device for a load fed via phase taps of at least two half-bridges, each of the half-bridges being controllable with a control of its own (Fig. 1, #s 13 control each half-bridge for each phase); each control comprising: a first electronic switch between the supply voltage and a phase tap (Fig. 1, Dm1); a second electronic switch between the phase tap and ground (Fig. 1, Dm2); a control circuit that controls the first and second switches, with one of only three switching signal pairings for the two electronic switches, and where the signal pairings are (1) the first switch on and the second switch off, (2) the first switch off and the second switch on, (3) and both switches off (cols. ½, ll. 60-67/1-2); and the control device comprising: a processor having a common signal output port coupled to control the controls via the respective control circuit of each control to select one of the three switching signal pairings, via one of three possible output signals at the common signal output port (Fig. 1, because INA is the only input from #12 to #13,this means that three

different signals make #13 control the switches, Dm1 & Dm2 operate in one of the three signal pairings; also note that if both transistors are turned on, the transistors would become damaged. Therefore, Genova et al disclose only three signal pairings).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fucili et al (5,886,484) and Genova et al (6,534,937), separately, as applied to claims 18 and 19 above, and further in view of Control Integrated Circuit Designers' Manual, IR211 – Half-Bridge Driver, 1996, page B-41 [hereinafter Designers' Manual].

- Neither Fucili et al nor Genova et al disclose the signal output port of the processor being at a feed voltage.
- The Designers' Manual discloses the input to a H-bridge driver (control circuit) being at the feed voltage of the control circuit (see "Static Electrical Characteristics"). This implies that the output port of a processor that feeds this driver is at the feed voltage of the control circuit. The motivation to make the output port of the processor at the feed voltage of the control circuit is to properly "bias" the driver.
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to make the output ports of Fucili et al and Genova et al at the feed

voltage of the control circuit, thereby providing the advantage of properly biasing the control circuit, as taught by the Designers' Manual.

5. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fucili et al (5,886,484) and Genova et al (6,534,937), separately, as applied to claims 18 and 21 above, and further in view of Chapman (6,232,731).

   - Neither Fucili et al nor Genova et al disclose the stage has hardwired components, which establishes fixed associations between the switching signal pairings and switching states.
   - Chapman discloses hard wiring the pattern of switching transitions within control electronics, which means fixed associations as well, as described above (col. 3, ll. 59-62). The motivation to provide hard-wired circuitry in the control electronics is to provide the advantage of a less complex circuit, as compared to circuitry that is reprogrammable or reconfigurable.
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to make the control circuit of Fucili et al or Genova et al hard-wired, which also means a fixed association, thereby providing the advantage of a less complex circuit, as compared to a circuit that is reprogrammable, as taught by Chapman.

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fucili et al (5,886,484) and Genova et al (6,534,937), separately, as applied to claims 18 and 25 above, and further in view of Control Integrated Circuit Designers' Manual, IR211 – Half-Bridge Driver, 1996, page B-41 [hereinafter Designers' Manual].

   - Neither Fucili et al nor Genova et al disclose the inputs of the complementary stages are connected to the signal output port via like-valued resistors.

- The Designers' Manual discloses an H-bridge driver that has a resistor at its input (see p. B-42, 'Functional Block Diagram'). This would make the resistor connected to the output port for each half-bridge of each phase. Furthermore, it would have been obvious that since each phase is the same, each driver would be the same, and thus, each resistor the same value. The motivation to use a resistor is to "pull" the voltage at the input of the driver low, so as to prevent the voltage at the input from "floating."
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the driver circuits of Fucili et al and Genova et al, like-valued resistors, thereby providing the advantage of preventing the voltage at the driver input from "floating," as taught by the Designers' Manual.

***Allowable Subject Matter***

7. Claims 28 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
   - With respect to claim 28, the Prior Art does not disclose the limitations of claim 18 and wherein in the event a feed voltage at the processor breaks down, the control circuit produces a switching signal pairing in which the first switch is switched off and the second switch is switched on. Note that feed voltage at the processor is interpreted to the feed voltage for the processor, as opposed to the voltage input from the processor to the control circuit.
   - With respect to claim 34, the Prior Art discloses operating a first switch of a half-bridge using pulse-width modulation, while keeping the corresponding second switch constantly

turned on. However, the Prior Art does not suggest motivation to combine this feature with a control device with the limitations of claims 32 and 33.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Miller whose telephone number is 571-272-2070. The examiner can normally be reached on M-F, 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on 571-272-2800 ext 41. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick Miller
Examiner
Art Unit 2837

pm
March 7, 2005

DAVID MARTIN
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